SQFlash SD Card Datasheet

(SQF-ISDx1-xG-21x)

CONTENTS

Revision History

Rev.	Date	History
0.1	2014/7/1	1. 1st draft
0.2	2015/7/1	1. Update to 15nm MLC
0.3	2016/3/10	1. Add ultra MLC and wear leveling information
0.4	2016/3/15	1. Add TBW information
0.5	2018/8/27	1. Update product temperature range
0.6	2018/11/12	1. Add low capacity solution
0.7	2019/3/24	1. Add temperature information
0.8	2020/2/15	1. Add power consumption
0.9	2020/6/15	1. Add power failure saver information
1.0	2020/7/6	1. Add power consumption
1.1	2022/1/22	1. Update TBW data

1. Overview

The Industrial SD Card (ISD) of the SQFlash is fully compliant to the specification released by SD Card Association. The Command List supports [Part 1 Physical Layer Specification Ver3.1 Final] definitions. Card Capacity of Non-secure Area, Secure Area Supports [Part 3 Security Specification Ver3.0 Final] Specifications.

The SQF-ISD is based on 9-pin interface, designed to operate at a maximum operating frequency of 100MHz. It can alternate communication protocol between the SD mode and SPI mode. It performs data error detection and correction with very low power consumption. Current capacity would be offered from 4GB to 64GB; it's possible to reach 2TB in the future with ex-FAT, which is called SDXC (Extended Capacity SD Memory Card).

The SQF-ISD is specifically made for any rigorous environments where devices need to be operated at extended temperature, and strong data integrity and reliability are demanded. Such environments include both industrial and automotive applications. The SQF-ISD is the best choice for exceptional reliability, excellent performance and wide compatibility.

2. Standard Features

- **Support SD system specification version 2.0 and 3.0. and compliant with UHS-I**
- **Card Capacity of Non-secure Area, Secure Area Supports [Part 3 Security Specification Ver3.0 Final] Specifications**
- **Support SD SPI mode**
- **Designed for read-only and read/write cards.**
- **The Command List supports [Part 1 Physical Layer Specification Ver3.01 Final] definitions**
- **Copyrights Protection Mechanism - Complies with highest security of SDMI standard**
- **CPRM (Content Protection for Recordable Media) of SD Card supported**
- **Support up to 72bits BCH ECC circuits to protect data communication.**
- **Global Wear Leveling support**
  - **SQFlash provides advanced Wear Leveling algorithm, which can efficiently spread out the flash usage through the whole flash media area. Moreover, by implementing both dynamic and static Wear Leveling algorithms, the life expectancy of the NAND Flash is greatly improved.**
- **Card removal during read operation will never harm the content**
- **Password Protection of cards (option)**
- **Write Protect feature using mechanical switch**
- **Built-in write protection features (permanent and temporary)**
- **High transmission speed**
- **+4KV/-4KV ESD protection in contact pads**
- **Dimensions: 32mm (L) x 24mm (W) x 2.1mm (H)**
- **Operating voltage range : 2.7-3.6V**

3. Additional Features

■ Capacities

- SLC type：128MB，256MB，512MB，1GB，2GB，4GB，8GB，16GB，32GB
- Ultra MLC type：2GB，4GB，8GB，16GB，32GB，64GB
- MLC type：4GB，8GB，16GB，32GB，64GB，128GB

■ Flash type

- SLC：32nm for 1G / 2G, the rest are 24nm
- MLC：15nm

■ Performance (MB per sec)

- Max. Read / Write: 90 / 45

■ Temperature Ranges

- Commercial Temperature
  - -25℃ to 85℃ for operating
  - -40℃ to 85℃ for storage
- Industrial Temperature
  - -40℃ to 85℃ for operating
  - -40℃ to 85℃ for storage

■ Mechanical Specification

- Shock：1,500G, Peak / 0.5ms
- Vibration：5G, Peak / 10~2000Hz
- Drop Test: 1.5m free fall
- Torque Test: 0.15N-m or +/-2.5deg
- Switch Cycles Test: Slide 0.4N to 5N

■ Humidity

- Operating Humidity：5% ~ 93%
- Non-Operating Humidity：5% ~ 93%

■ NAND flash Data Retention

- 10 years

Endurance

JEDEC defined an endurance rating TBW (TeraByte Written), following by the equation below, for indicating the number of terabytes a flash drive can be written which is a measurement of flash drive's expected lifespan, represents the amount of data written to the device.

TBW = [(NAND Endurance) x (Flash Drive Capacity)] / WAF

- **NAND Endurance**: Program / Erase cycle of a NAND flash.
  - SLC: 60,000 cycles
  - Ultra MLC: 20,000 cycles
  - MLC: 3,000 cycles
- **Flash Drive Capacit**y: Physical capacity in total of a Flash Drive.
- **WAF**: Write Amplification Factor (WAF), as the equation shown below, is a numerical value representing the ratio between the amount of data that a flash drive controller needs to write and the amount of data that the host's flash controller writes. A better WAF, which is near to 1, guarantees better endurance and lower frequency of data written to flash memory.

WAF = (Lifetime write to flash) / (Lifetime write to host)

The TBW rating for a flash drive shall be derived for and verified under the following workload conditions,

- Sequential Write (copy file into card)
- P/E cycles incurred: erase count after writing – erase count before writing

➢ **SQFlash SD Card TBW**

	TBW		
	SLC	Ultra MLC	MLC
1 GB	58	--	--
2 GB	117	39	--
4 GB	234	77	11
8 GB	469	155	23
16 GB	937	310	47
32 GB	1874	621	93
64 GB	--	1243	186
128 GB	--	--	372

4. General Description

■ Power Failure Saver : Data Integrity Check

When the controller IC is writing data and suddenly the power fails, the controller IC will judge if it has completed one full page of written data before power failure; If not, the data of this incomplete page will be flagged as having failed. The controller IC will then implement a recovery mechanism in F/W, and after powering up, it will check the data written in the flash previously, if the data has been detected as invalid it drops the invalid part, then merges the old valid data with the newer valid data to make a new combination of data that are all valid. This will eliminate the chance of getting wrong data caused by non-complete writing to flash.

5. Pin Assignment and Block Diagram

SD memory Card Pad Assignment

pin	SD Mode			SPI Mode		
	Name	**Type (1)**	**Description**	**Name**	**Type**	**Description**
1	CD/DAT3 **(2)**	I/O/PP (3)	Card Detect/ Data Line[bit3]	CS	I (3)	Chip Select (net true)
2	CMD	PP	Command/Response	DI	I	Data In
3	V_{SS1}	S	Supply voltage ground	VSS	S	Supply voltage ground
4	V_{DD}	S	Supply voltage	VDD	S	Supply voltage
5	CLK	I	Clock	SCLK	I	Clock
6	V_{SS2}	S	Supply voltage ground	VSS2	S	Supply voltage ground
7	DAT0	I/O/PP	Data Line[bit0]	DO	O/PP	Data Out
8	DAT1	I/O/PP	Data Line[bit1]	RSV		
9	DAT2	I/O/PP	Data Line[bit2]	RSV		

(1) S: power supply, I:input; O:output using push-pull drivers; PP:I/O using push-pull drivers

(2) The extended DAT lines (DAT1-DAT3) are input on power up. They start to operate as DAT lines after SET_BUS_WIDTH command. The Host shall keep its own DAT1-DAT3 lines in input mode, as well, while they are not used. It is defined so, in order to keep compatibility to MultiMedia Cards.

(3) At power up this line has a 50KOhm pull up enabled in the card. This resistor serves two functions Card detection and Mode Selection. For Mode Selection, the host can drive the line high or let it be pulled high to select SD mode. If the host wants to select SPI mode it should drive the line low. For Card detection, the host detects that the line is pulled high. This pull-up should be disconnected by the user, during regular data transfer, with SET_CLR_CARD_DETECT (ACMD42) command.

Name	Width	Description
CID	128bit	Card identification number; card individual number for identification. **Mandatory**
RCA	16bit	Relative card address; local system address of a card, dynamically suggested by the card and approved by the host during initialization. **Mandatory**
DSR	16bit	Driver Stage Register; to configure the card's output drivers. **Optional**
CSD	128bit	Card Specific Data; information about the card operation conditions. **Mandatory**
SCR	64bit	SD Configuration Register; information about the SD Memory Card's Special Features capabilities. **Mandatory**
OCR	32bit	Operation condition registers. **Mandatory**
SSR	512bit	SD Status; information about the card proprietary features. **Mandatory**
OCR	32bit	Card Status; information about the card status. **Mandatory**

6. Power Consumption

Table list as below is the power consumption of ISD card with different type of flash memory.
MLC type

Capacity	Read (mA)	Write (mA)	Idle (uA)
4 GB	80	90	0.2
8 GB	80	80	0.2
16 GB	80	80	0.2
32 GB	100	100	0.2
64 GB	100	100	0.2
128 GB	120	130	0.2

Ultra MLC type

Capacity	Read (mA)	Write (mA)	Idle (uA)
2 GB	80	90	0.2
4 GB	80	80	0.2
8 GB	80	80	0.2
16 GB	100	100	0.2
32 GB	100	100	0.2
64 GB	120	130	0.2

SLC type

Capacity	Read (mA)	Write (mA)	Idle (uA)
128 MB	40	50	0.2
256 MBB	40	50	0.2
512 MB	40	50	0.2
1 GB	50	60	0.2
2 GB	60	80	0.2
4 GB	40	50	0.2
8 GB	50	60	0.2
16 GB	60	80	0.2
32 GB	70	110	0.2

(1) Data transfer mode is single channel.
(2) Power Consumption may differ according to flash configuration, SDR configuration, or platform.

7. DC Characters

7.1 BUS Operating Conditions for 3.3V Signaling

Threshold level for High Voltage Range

Parameter	Symbol	Min	Max	Unit	Remarks
Supply voltage	V_{DD}	2.7	3.6	V	
Output High Voltage	VOH	0.75*VDD		V	IOH=-100uA V_{DD}Min.
Output Low Voltage	VOL		0.125*VDD	V	IOL = 100uA V_{DD}min
Input High Voltage	VIH	0.625*VDD	VDD+0.3	V	
Input Low Voltage	VIL	VSS-0.3	0.25 *VDD	V	
Power up time			250	ms	From 0v to V_{DD}min.

Peak Voltage and Leakage Current

Parameter	Symbol	Min	Max	Unit	Remarks
Peak voltage on all lines		-0.3	V_{DD}+0.3	V	
All Inputs					
Input Leakage Current		-10	10	uA	
All Outputs					
Output Leakage Current		-10	10	uA	

Threshold Level for 1.8V Signaling

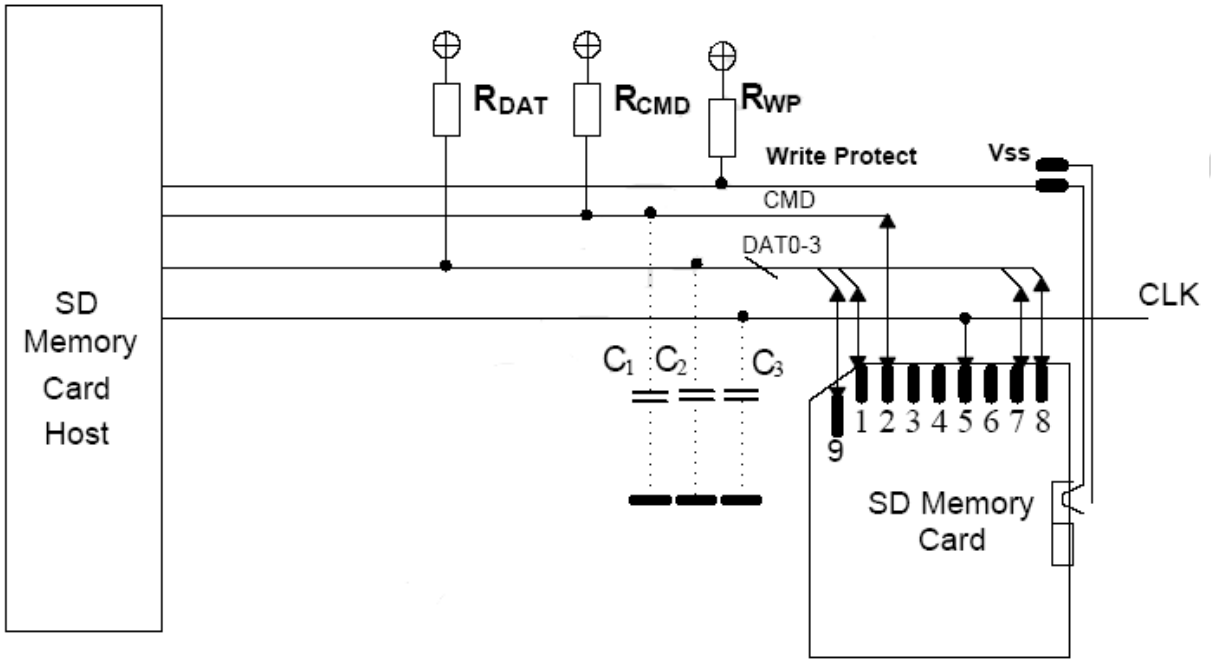
Parameter	Symbol	Min	Max	Unit	Condition
Supply Voltage	V_{DD}	2.7	3.6	V	
Regulator Voltage	V_{DDIO}	1.7	1.95	V	Generated by V_{DD}
Output High Voltage	VOH	1.4	-	V	IOH = -2mA
Output Low Voltage	VOL		0.45	V	IOL = 2mA
Input High Voltage	VIH	1.27	2.00	V	
Input Low Voltage	VIL	V_{ss} – 0.3	0.58	V	

Input Leakage Current for 1.8V Signaling

Parameter	Symbol	Min	Max	Unit	Remarks
Input Leakage Current		-2	2	uA	DAT3 pull-up isdisconnected.

BUS Operating Conditions for 3.3V Signaling

BUS Circuitry Diagram:



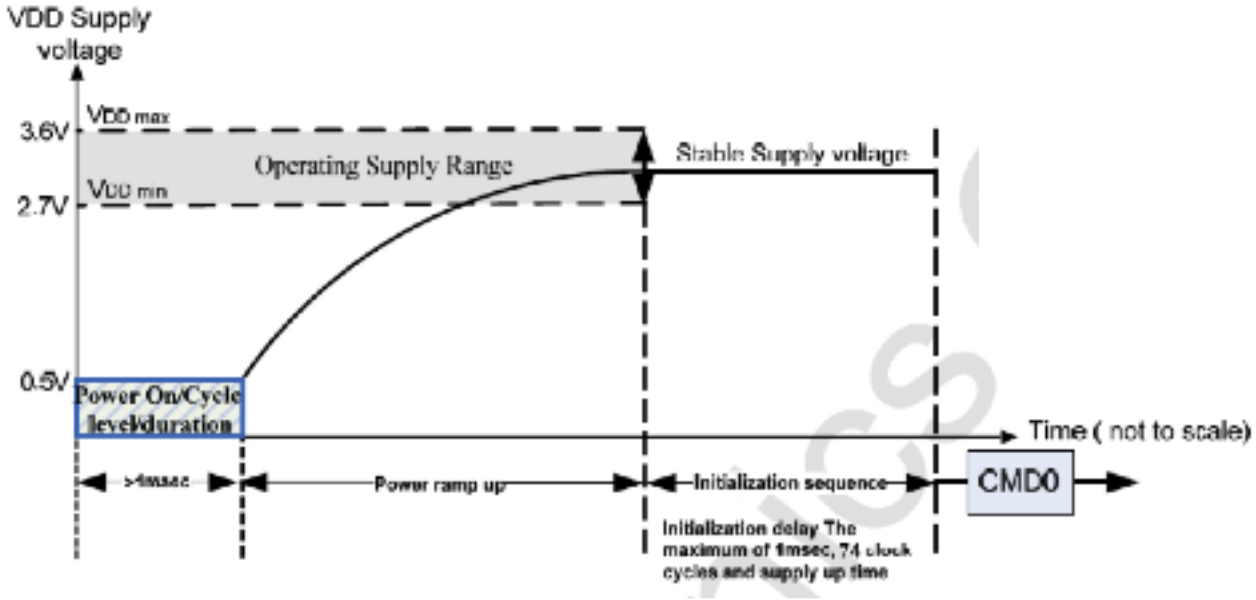
BUS Operating Conditions – Signal Line's Load

Total bus cpapcitance = CHOST + CBUS + N CCARD

Parameter	Symbol	Min	Max	Unit	Remark
Pull-up resistance	R_{CMD} R_{DAT}	10	100	kΩ	to prevent bus floating
Total bus capacitance for each signal line	C_L		40	pF	1 card CHOST+CBUS shall not exceed 30 pF
Capacitance of the card for each signal pin	C_{CARD}		10	pF	
Maximum signal line inductance			16	nH	
Pull-up resistance inside card (pin1)	R_{DAT3}	10	90	kΩ	May be used for card detection
Caoacity Connected to Power Line	C_C		5	uF	To prevent inrush current

7.2 Power Up Time

Host needs to keep power line level less than 0.5V and more than 1ms before power ramp up.



Power On or Power Cycle

Followings are requirements for Power on and Power cycle to assure a reliable SD Card hard reset.

(1) Voltage level shall be below 0.5V

(2) Duration shall be at least 1ms.

Power Supply Ramp Up

The power ramp up time is defined from 0.5V threshold level up to the operating supply voltage which is stable between VDD(min.) and VDD(max.) and host can supply SDCLK.

Followings are recommendation of Power ramp up:

(1) Voltage of power ramp up should be monotonic as much as possible.

(2) The minimum ramp up time should be 0.1ms.

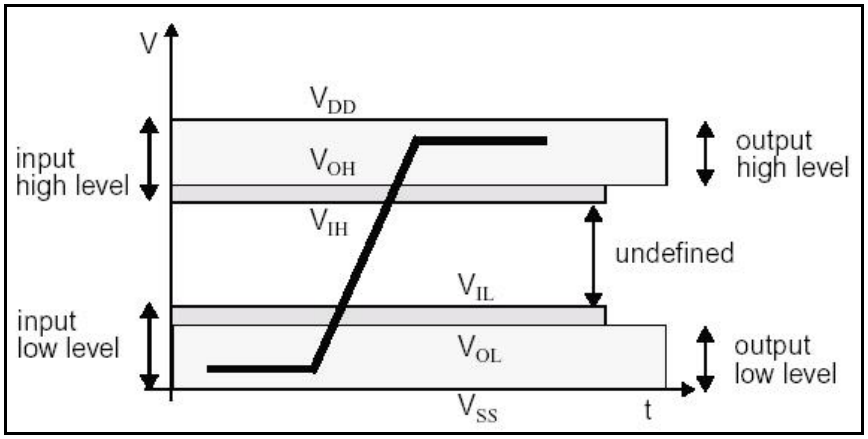
(3) The maximum ramp up time should be 35ms for 2.7-3.6V power supply.

Power Down and Power Cycle

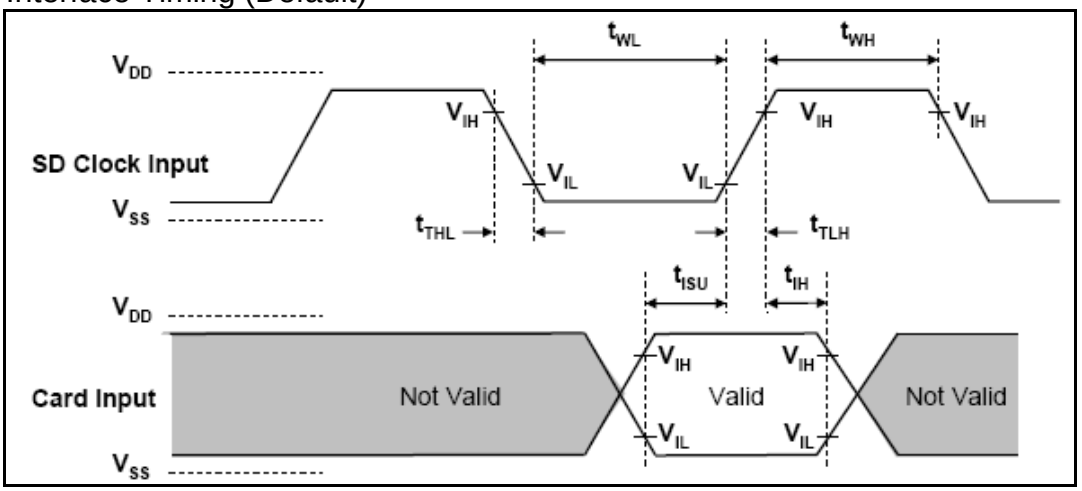
• When the host shuts down the power, the card VDD shall be lowered to less than 0.5Volt for a minimum period of 1ms. During power down, DAT, CMD, and CLK should be disconnected or driven to logical 0 by the host to avoid a situation that the operating current is drawn through the signal lines.

• If the host needs to change the operating voltage, a power cycle is required. Power cycle means the power is turned off and supplied again. Power cycle is also needed for accessing cards that are already in Inactive State. To create a power cycle the host shall follow the power down description before power up the card (i.e. the card VDD shall be once lowered to less than 0.5Volt for a minimum period of 1ms).

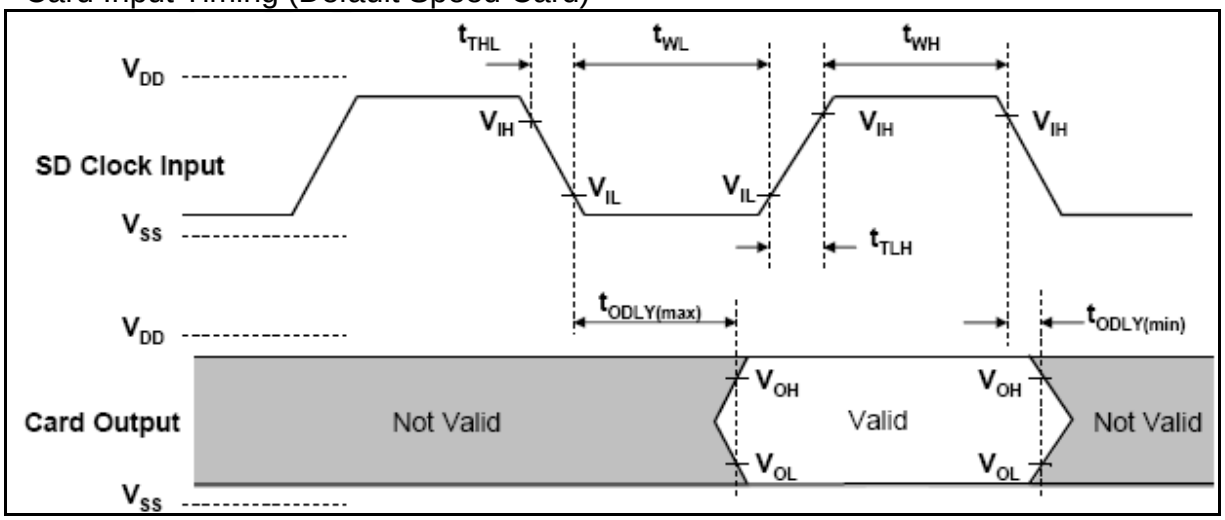
8. AC Characters



8.1 SD Interface Timing (Default)



8.2 Card Input Timing (Default Speed Card)

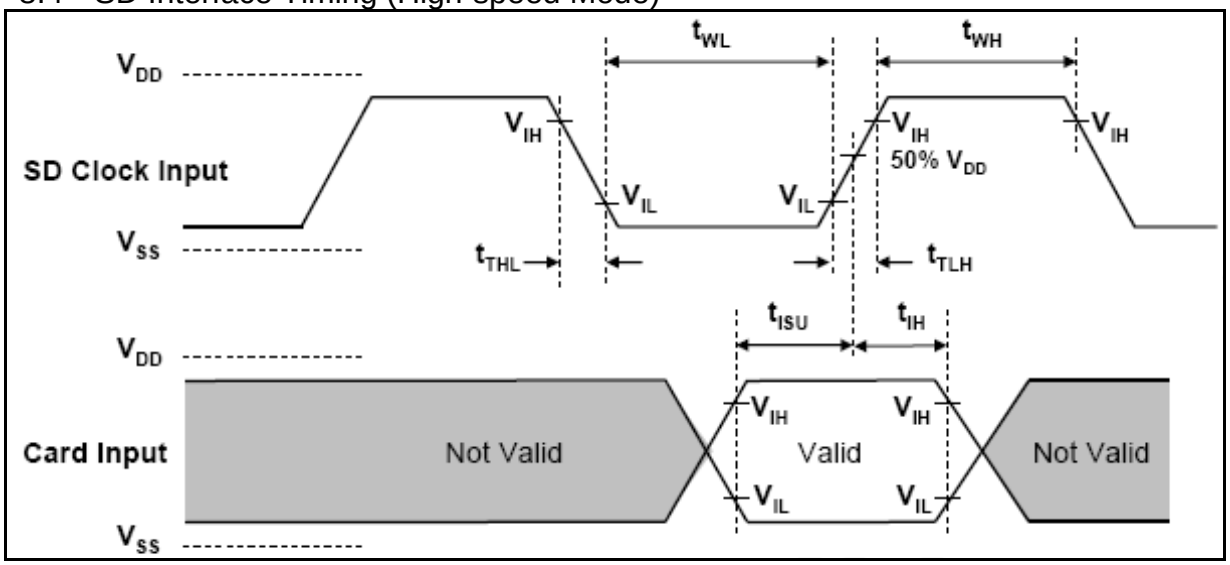


8.3 Card Output Timing (Default Speed Mode)

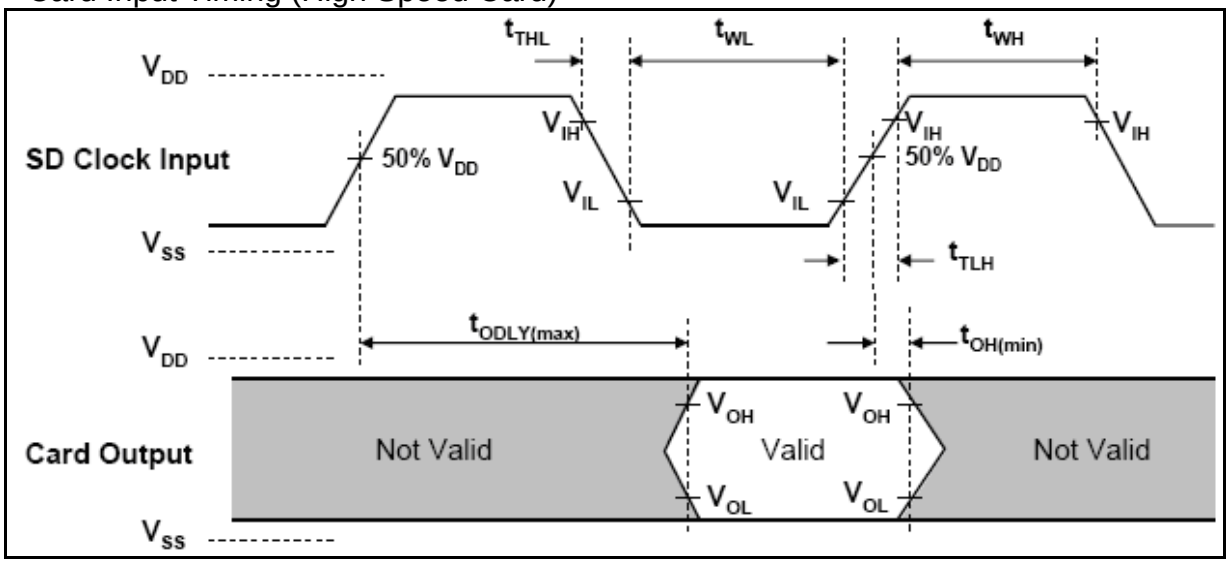
Parameter	Symbol	Min	Max	Unit	Remark
Clock CLK (All values are referred to min(V_{IH}) and max(V_{IL})					
Clock frequency Data Transfer Mode	f_{PP}	0	25	MHz	C_{card}≤ 10 pF (1 card)
Clock frequency Identification Mode	f_{OD}	0(1)/100	400	kHz	C_{card}≤ 10 pF (1 card)
Clock low time	t_{WL}	10		ns	C_{card}≤ 10 pF (1 card)
Clock high time	t_{WH}	10		ns	C_{card}≤ 10 pF (1 card)
Clock rise time	t_{TLH}		10	ns	C_{card}≤ 10 pF (1 card)
Clock fall time	t_{THL}		10	ns	C_{card}≤ 10 pF (1 card)
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	5		ns	C_{card}≤ 10 pF (1 card)
Input hold time	t_{IH}	5		ns	C_{card}≤ 10 pF (1 card)
Outputs CMD, DAT (referenced to CLK)					
Output Delay time during Data Transfer Mode	t_{ODLY}	0	14	ns	C_L≤40 pF (1 card)
Output Delay time during Identification Mode	tODLY	0	50	ns	C_L≤40 pF (1 card)

0Hz means to stop the clock. The given minimum frequency range is for cases were continues clock is required.

8.4 SD Interface Timing (High-speed Mode)



8.5 Card Input Timing (High Speed Card)



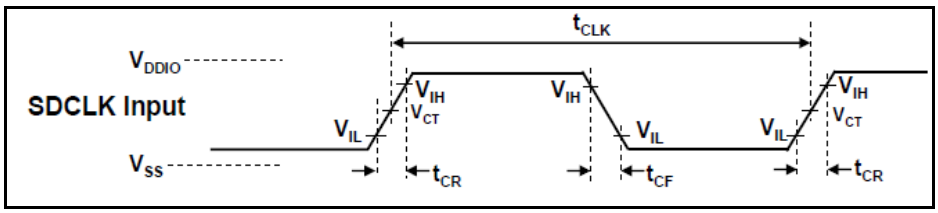
8.6 Card Output Timing (Default Speed Mode)

Parameter	Symbol	Min	Max	Unit	Remark
Clock CLK (All values are referred to min(V_{IH}) and max(V_{IL})					
Clock frequency Data Transfer Mode	f_{PP}	0	50	MHz	C_{card}≤ 10 pF (1 card)
Clock low time	t_{WL}	7		ns	C_{card}≤ 10 pF (1 card)
Clock high time	t_{WH}	7		ns	C_{card}≤ 10 pF (1 card)
Clock rise time	t_{TLH}		3	ns	C_{card}≤ 10 pF (1 card)
Clock fall time	t_{THL}		3	ns	C_{card}≤ 10 pF (1 card)
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	6		ns	C_{card}≤ 10 pF (1 card)
Input hold time	t_{IH}	2		ns	C_{card}≤ 10 pF (1 card)
Outputs CMD, DAT (referenced to CLK)					
Output Delay time during Data Transfer Mode	t_{ODLY}		14	ns	C_L≤40 pF (1 card)
Output Hold time	T_{OH}	2.5	50	ns	C_L≤15 pF (1 card)
Total System capacitance of each line[1]	C_L		40	pF	CL≤15 pF card)

In order to satisfy severe timing, host shall drive only one card.

8.7 SD Interface timing (SDR12, SDR25 and SDR50 Modes)

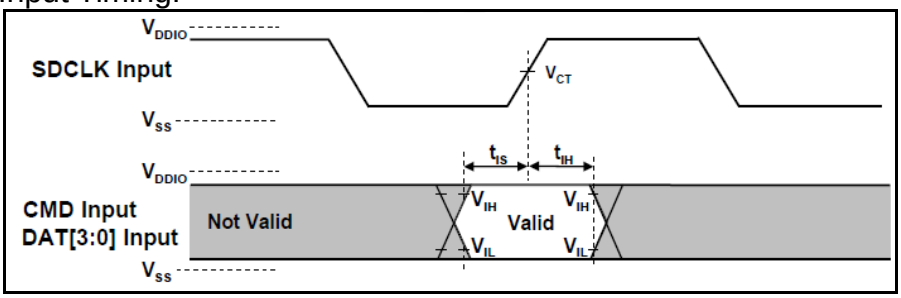
Input:



Symbol	Min	Max	Unit	Remark
tCLK	4.80	0	ns	208MHz (Max.), Between rising edge, VCT= 0.975V
tCR, tCF	-	0.2 * tCLK	ns	tCR, tCF < 2.00ns (max.) at 100MHz, CCARD=10pF
Clock Duty	30	70	%	

8.8 Clock Signal Timing

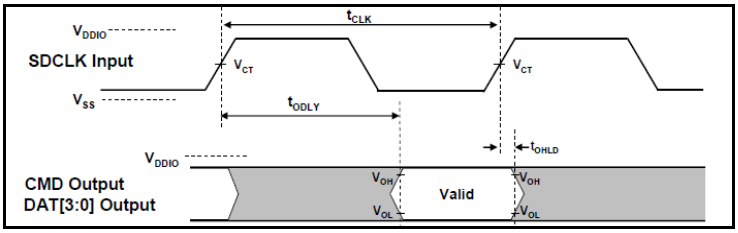
SDR50 Input Timing:



Symbol	Min	Max	Unit	Remark
tIs	3.00	-	ns	C_{CARD} =10pF, VCT= 0.975V
tIH	0.80	-	ns	C_{CARD} =5pF, VCT= 0.975V

8.9 Card Input Timing

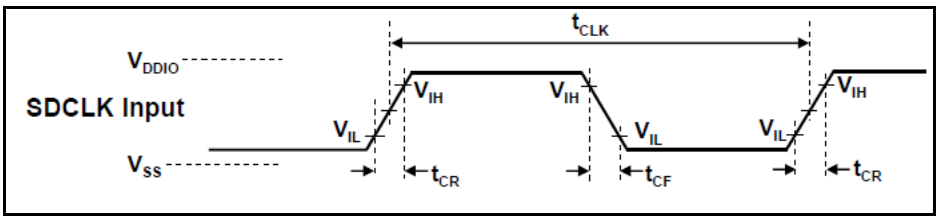
Output:



Symbol	Min	Max	Unit	Remark
tODLY	-	7.5	ns	tCLK>=10.0ns, CL=30pF, using driver Type B, for SDR50
tODLY	-	14	ns	tCLK>=20.0ns, CL=40pF, using driver Type B, for SDR25 and SDR12,
TOH	1.5	-	ns	Hold time at the tODLY (min.), CL=15pF

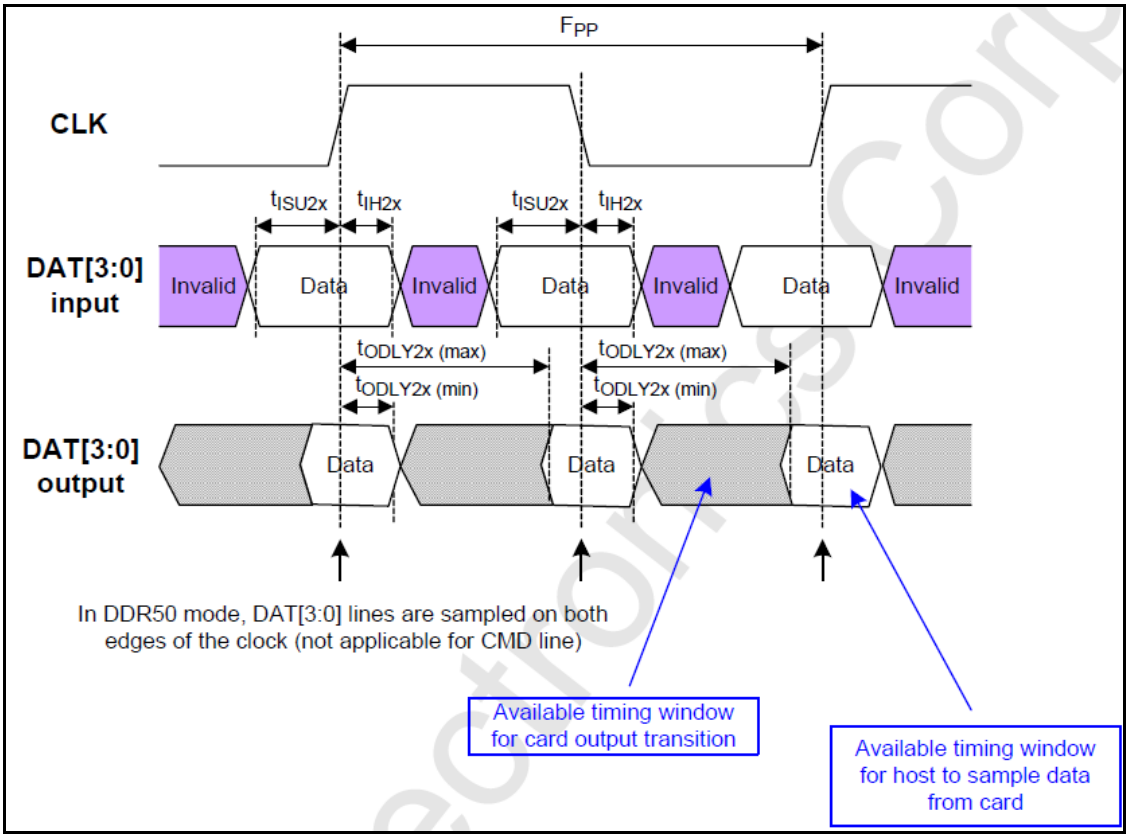
8.10 Output Timing of Fixed Data Window

SD Interface timing (DDR50 Modes)



Symbol	Min	Max	Unit	Remark
tCLK	20	-	ns	50MHz (Max.), Between rising edge
tCR, tCF	-	0.2 * tCLK	ns	tCR, tCF < 4.00ns (max.) at 50MHz, CCARD=10pF
Clock Duty	45	55	%	

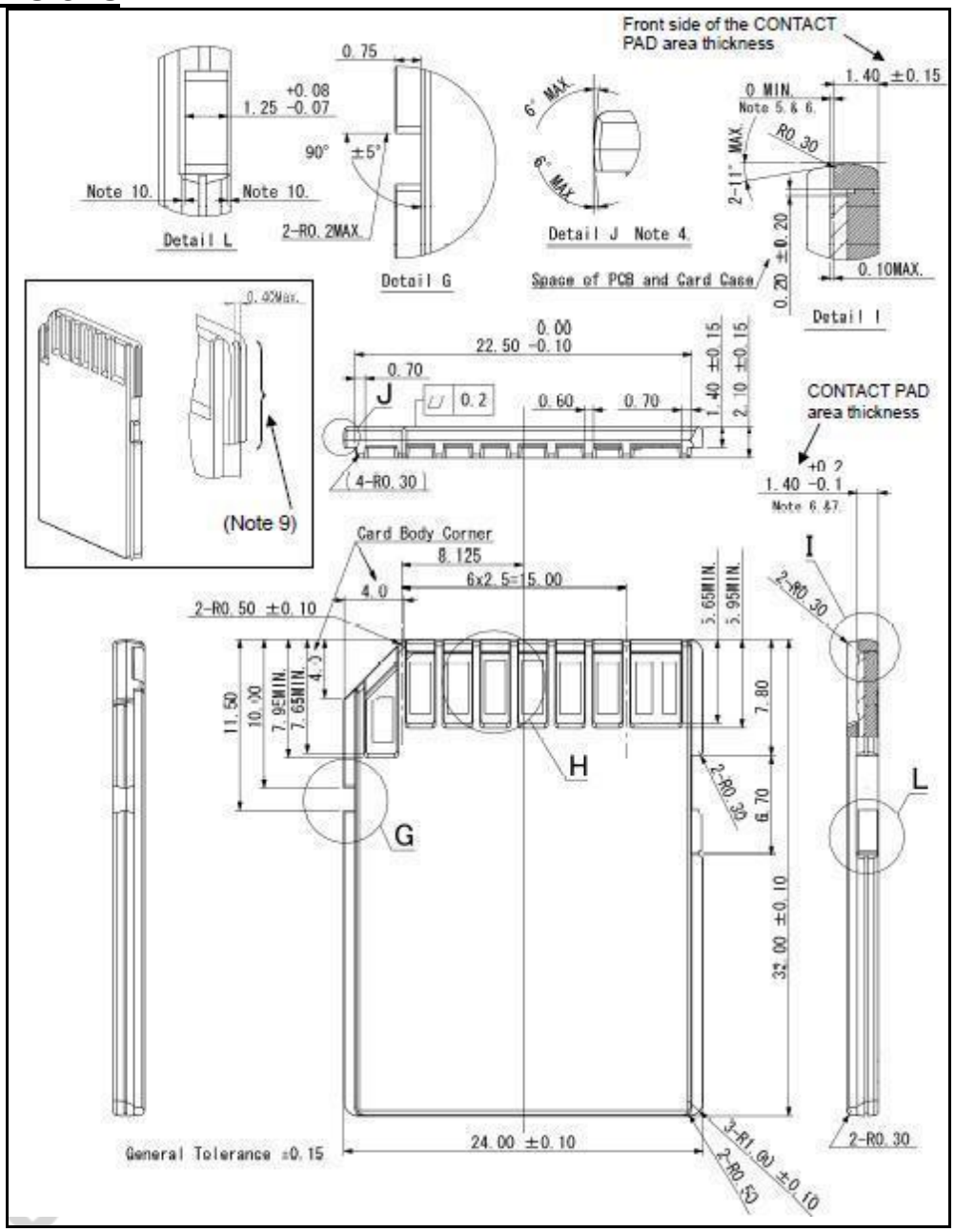
8.11 Clock Signal Timing



Timing Diagram DAT Inputs / Outputs Referenced to CLK in DDR50 Mode

Parameter	Symbol	Min	Max	Unit	Remark
Input CMD (referenced to CLK rising edge)					
Input set-up time	t_{ISU}	6	-	ns	C_{card}≤ 10 pF (1 card)
Input hold time	t_{IH}	0.8	-	ns	C_{card}≤ 10 pF (1 card)
Output CMD (referenced to CLK rising edge)					
Output Delay time during Data Transfer Mode	t_{ODLY}		13.7	ns	C_{card}≤ 30 pF (1 card)
Output Hold time	t_{OH}	1.5	-	ns	C_{card}≤ 10 pF (1 card)
Inputs DAT (referenced to CLK rising and falling edges)					
Input set-up time	t_{ISU2X}	3	-	ns	C_{card}≤ 10 pF (1 card)
Input hold time	t_{IH2X}	0.8	-	ns	C_{card}≤ 10 pF (1 card)
Outputs CMD, DAT (referenced to CLK)					
Output Delay time during Data Transfer Mode	t_{ODLY2X}	-	7.0	ns	C_L≤25 pF (1 card)
Output Hold time	t_{OH2X}	1.5	-	ns	C_L≥15 pF (1 card)

9. Dimensions



Dimensions of A SD Card (Bottom View, DIN)

Appendix: Part Number Table

SLC

Product	Advantech PN
SQF I-SD C6 SLC 128M (-25~85°C)	SQF-ISDS1-128M-21C
SQF I-SD C6 SLC 256M (-25~85°C)	SQF-ISDS1-256M-21C
SQF I-SD C6 SLC 512M (-25~85°C)	SQF-ISDS1-512M-21C
SQF I-SD C6 SLC 1G (-25~85°C)	SQF-ISDS1-1G-21C
SQF I-SD C6 SLC 2G (-25~85°C)	SQF-ISDS1-2G-21C
SQF I-SD C6 SLC 4G (-25~85°C)	SQF-ISDS1-4G-21C
SQF I-SD C10 SLC 8G (-25~85°C)	SQF-ISDS1-8G-21C
SQF I-SD C10 SLC 16G (-25~85°C)	SQF-ISDS1-16G-21C
SQF I-SD C10 SLC 32G (-25~85°C)	SQF-ISDS1-32G-21C
SQF I-SD C6 SLC 128M (-40~85°C)	SQF-ISDS1-128M-21E
SQF I-SD C6 SLC 256M (-40~85°C)	SQF-ISDS1-256M-21E
SQF I-SD C6 SLC 512M (-40~85°C)	SQF-ISDS1-512M-21E
SQF I-SD C6 SLC 1G (-40~85°C)	SQF-ISDS1-1G-21E
SQF I-SD C6 SLC 2G (-40~85°C)	SQF-ISDS1-2G-21E
SQF I-SD C6 SLC 4G (-40~85°C)	SQF-ISDS1-4G-21E
SQF I-SD C10 SLC 8G (-40~85°C)	SQF-ISDS1-8G-21E
SQF I-SD C10 SLC 16G (-40~85°C)	SQF-ISDS1-16G-21E
SQF I-SD C10 SLC 32G (-40~85°C)	SQF-ISDS1-32G-21E

Ultra MLC

Product	Advantech PN
SQF I-SD UHS-I UMLC 4G (-25~85°C)	SQF-ISDU1-4G-21C
SQF I-SD UHS-I UMLC 8G (-25~85°C)	SQF-ISDU1-8G-21C
SQF I-SD UHS-I UMLC 16G (-25~85°C)	SQF-ISDU1-16G-21C
SQF I-SD UHS-I UMLC 32G (-25~85°C)	SQF-ISDU1-32G-21C
SQF I-SD UHS-I UMLC 64G (-25~85°C)	SQF-ISDU1-64G-21C
SQF I-SD UHS-I UMLC 4G (-40~85°C)	SQF-ISDU1-4G-21E
SQF I-SD UHS-I UMLC 8G (-40~85°C)	SQF-ISDU1-8G-21E
SQF I-SD UHS-I UMLC 16G (-40~85°C)	SQF-ISDU1-16G-21E
SQF I-SD UHS-I UMLC 32G (-40~85°C)	SQF-ISDU1-32G-21E
SQF I-SD UHS-I UMLC 64G (-40~85°C)	SQF-ISDU1-64G-21E

MLC

Product	Advantech PN
SQF I-SD UHS-I MLC 4G (-25~85°C)	SQF-ISDM1-4G-21C
SQF I-SD UHS-I MLC 8G (-25~85°C)	SQF-ISDM1-8G-21C
SQF I-SD UHS-I MLC 16G (-25~85°C)	SQF-ISDM1-16G-21C
SQF I-SD UHS-I MLC 32G (-25~85°C)	SQF-ISDM1-32G-21C
SQF I-SD UHS-I MLC 64G (-25~85°C)	SQF-ISDM1-64G-21C
SQF I-SD UHS-I MLC 128G (-25~85°C)	SQF-ISDM1-128G-21C
SQF I-SD UHS-I MLC 4G (-40~85°C)	SQF-ISDM1-4G-21E
SQF I-SD UHS-I MLC 8G (-40~85°C)	SQF-ISDM1-8G-21E
SQF I-SD UHS-I MLC 16G (-40~85°C)	SQF-ISDM1-16G-21E
SQF I-SD UHS-I MLC 32G (-40~85°C)	SQF-ISDM1-32G-21E
SQF I-SD UHS-I MLC 64G (-40~85°C)	SQF-ISDM1-64G-21E
SQF I-SD UHS-I MLC 128G (-40~85°C)	SQF-ISDM1-128G-21E